In the Claims:

Please cancel claims 12 and 19-21, without prejudice, and amend claims 1 and 22 as follows:

1. (Currently Amended) A processor comprising:

a plurality of pipelines, each pipeline having a plurality of pipeline stages for executing an instruction on successive clock cycles; and

stall control circuitry which controls the stalling of instructions in the pipelines in response to a stall signal generated in any one of the pipelines; ~~wherein~~

the stall control circuitry being adapted to stall the execution of an instruction in a pipeline not generating the stall signal at least one clock cycle later than the execution of an instruction in a pipeline generating the stall signal, and to release the stall in the pipeline not generating the stall signal at least one clock cycle later than the stall in the pipeline generating the stall signal,

wherein all the pipelines have substantially the same instruction-processing capability and are not flushed in response to the stall signal.

2. (Original) A processor according to claim 1 wherein the stall control circuitry is arranged such that, when a pipeline stage in a first pipeline receives a stall signal from a second pipeline, the execution of instructions in the pipeline stage in the first pipeline is not stalled if that pipeline stage stalled in the previous cycle in response to a stall signal generated by the first pipeline.

3. (Original) A processor according to claim 1 wherein the stall control circuitry is arranged such that, when a pipeline generates a stall signal at a stage i, all stages up to and including stage i of that pipeline are stalled.

4. (Original) A processor according to claim 1 wherein, when a pipeline generates a stall signal at a stage i, all stages up to and including stage i of that pipeline are stalled on a given clock cycle, and all stages up to and including stage i+m of a pipeline not generating a stall signal are stalled m clock cycles later than said given clock cycle, where m is an integer greater than or equal to 1.

5. (Original) A processor according to claim 1 wherein the processor comprises a plurality of pipeline clusters, each cluster comprising a plurality of pipelines.

6. (Original) A processor according to claim 5 wherein the stall control circuitry is arranged to stall execution of instructions in pipelines within a cluster in the same clock cycle.

7. (Original) A processor according to claim 5 wherein the stall control circuitry is arranged to stall the execution of instructions in pipelines in a cluster not generating the stall signal at least one clock cycle later than the execution of instructions in pipelines in a cluster generating the stall signal.

8. (Original) A processor according to claim 1 wherein, in operation, instructions entering the respective pipelines in parallel exit the pipelines in parallel.

9. (Original) A processor according to claim 1 wherein, in operation, different instructions are executed in different pipelines.

10. (Original) A processor according to claim 1, being a VLIW processor in which instructions from a VLIW instruction packet are issued in parallel to the pipelines.

11. (Original) A processor according to claim 1 wherein each pipeline includes at least one execute stage in which an instruction is at least partially executed.

12. (Cancelled)

13. (Original) A processor according to claim 1 wherein the stall control circuitry is distributed between two or more pipeline stages.

14. (Original) A processor according to claim 1 wherein two or more pipeline stages each have associated stall control circuitry for controlling the stalling of that pipeline stage.

15. (Original) A processor according to claim 14 wherein the stall control circuitry in each pipeline stage is arranged to generate a global stall signal for stalling another pipeline, and to receive a global stall signal from another pipeline for stalling the pipeline stage with which the circuitry is associated.

16. (Original) A processor according to claim 15 wherein the stall control circuitry does not generate a global stall signal if the associated pipeline stage is subject to a global stall from the same stage or later in another pipeline.

17. (Original) A processor according to claim 14 wherein the stall control circuitry in each of the two or more pipelines is substantially the same.

18. (Original) A processor according to claim 1 wherein a pipeline stage is not stalled if there is a bubble in that pipeline stage.

19-21. (Cancelled)

22. (Currently Amended) A method of operating a processor, the processor comprising a plurality of pipelines, each pipeline having a plurality of pipeline stages for executing instructions on successive clock cycles, each pipeline being capable of generating a stall signal, and all the pipelines having substantially the same instruction- processing capability, the method comprising:

generating a stall signal in one of the pipelines;

stalling the execution of an instruction in the pipeline generating the stall signal and stalling the execution of an instruction in a pipeline not generating the stall signal at least one clock cycle later, wherein the pipeline generating the stall and pipeline not generating the stall are not flushed after being stalled;

releasing the stall in the pipeline generating the stall signal; and

releasing the stall in the pipeline not generating the stall signal at least one clock cycle later.